FORM PTO-1390 (Modified) (REV 10-95) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 990326

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5): 09/319699

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE97/02908	8 December 1997	9 December 1996

TITLE OF INVENTION

Silicon Germanium Hetero Bipolar Trasnsitor and Method of Making the Epitaxial Individual Layers of such a Transistor

APPLICANT(S) FOR DO/EO/US

Lippert et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U S.C 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ have been transmitted by the International Bureau.
   c. ☐ have not been made, however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3))
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 18 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
    A **SECOND** or **SUBSEQUENT** preliminary amendment.
16. ☐ A substitute specification.
17. ☐ A change of power of attorney and/or address letter.
18. ☒ Certificate of Mailing by Express Mail
19. ☒ Other items or information:

a.) a translation of the Specification and Claims as Amended before the International Preliminary Examniation Austaurity;
b.) a Post Card Receipt

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/319699	PCT/DE97/02908	990326

20. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☒	Search Report has been prepared by the EPO or JPO	**$840.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482)	**$670.00**
☐	No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2))	**$760.00**
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO	**$970.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)	**$96.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$840.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1 492 (e))	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	13 - 20 =	0	x $18.00	**$0.00**	
Independent claims	2 - 3 =	0	x $78.00	**$0.00**	
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS			=	**$840.00**	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**			☒	**$420.00**	
SUBTOTAL			=	**$420.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	**$0.00**	
TOTAL NATIONAL FEE			=	**$420.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☒	**$40.00**	
TOTAL FEES ENCLOSED			=	**$460.00**	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$460.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed

☐ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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Karl Hormann

NAME

26,470

REGISTRATION NUMBER

9 June 1999

DATE

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

PCT/DE97/02908
International Filing Date: 8 December 1997
Priority Date: 9 December 1996
Inventors: Lippert et al.
For: Silicon Germanium Hetero Bipolar Transistor and Method of Making the Epitaxial Individual Layers of such a Transistor

86 Sparks Street
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8 June 1999

Hon.
Assistant Commissioner
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Box PCT
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Preliminary Amendment Prior Claims Fee Calculation

Sir:

With a view to putting the English translation of instant International Application as amended before the International Preliminary Examination Authority into formal compliance with current U.S. patent prosecution practice and to avoiding excess claims fees otherwise due, Applicants courteously request that the following amendment be entered.

In the Specification

Page 1, line 8: enter --BACKGROUND OF THE INVENTION.

1. Field of the Invention.--;

line 20: enter --2. The Prior Art.--;

page 2, line 32: enter --OBJECTS OF THE INVENTION.--;

page 3, line 21: enter --SUMMARY OF THE INVENTION.--;

page 5, line 16: enter --DESCRIPTION OF THE SEVERAL DRAWINGS.--;

line 25: enter --DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS.--;

page 9, line 1: change "Patent Claims." to --What is claimed is:--; and

page 12, line 5: after "abstract" insert --of the Disclosure--.

In the Claims:

claim 3, line 2: cancel "1 or";

claim 4, line 2: change "one or more of the preceding claims" to --claim 1--;

claim 5, line 2: change "one or more of the preceding claims" to --claim 1--;

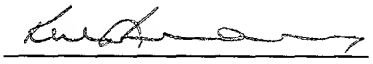
claim 10, line 1: change "one of claims 7 to" to --claim--;

claim 11, line 1: change "one or more of the claims 7 to" to --claim--;

claim 12, line 1: change "one or more of the claims 7 to" to --claim--; and

claim 13, line 1: change "one or more of the claims 7 to" to --claim--.

Respectfully submitted,



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Registration No.: 26,470

Area Code (617)-491-8867

IHP 095. PCT

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) AND 1.27 (c)) - SMALL BUSINESS CONCERN	Docket No. 990326

Serial No.	Filing Date	Patent No.	Issue Date
	9 June 1999		

Applicant/ Patentee: **LIPPERT et al.**

Invention: **Silicon Germanium Hetero Bipolar Transistor and Method of Fabricating the Epitactic Layers Thereof**

I hereby declare that I am:

- ☐ the owner of the small business concern identified below:
- ☒ an official of the small business concern empowered to act on behalf of the concern identified below:

INSTITUT FÜR HALBLEITERPHYSIK FRANKFURT (ODER) GmbH
Institut der WG Blaue Liste
PSF 409, 15204 Frankfurt (Oder) — Walter-Korsing-Straße 2, 15230 Frankfurt (Oder)
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NAME OF CONCERN: **Institut fuer Halbleiterphysik Frankfurt (Oder) GmbH.**

ADDRESS OF CONCERN: **Walter-Korsing-Strasse 2, D-15230 Frankfurt/Oder, Germany**

I hereby declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the above identified invention described in:

- ☒ the specification filed herewith with title as listed above.
- ☐ the application identified above.
- ☐ the patent identified above.

If the rights held by the above-identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed on the next page and no rights to the invention are held by any person, other than the inventor, who could not qualify as an independent inventor under 37 CFR 1.9(c) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- [x] no such person, concern or organization exists.
- [ ] each such person, concern or organization is listed below.

FULL NAME _____
ADDRESS _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

FULL NAME _____
ADDRESS _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

FULL NAME _____
ADDRESS _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

FULL NAME _____
ADDRESS _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: Prof. Abbas Ourmazd Franz Weinl

TITLE OF PERSON SIGNING: Scientific Director Administrative Director

OTHER THAN OWNER:

ADDRESS OF PERSON SIGNING: IHP Frankfurt (Oder) GmbH
Walter-Korsing-Str. 2
15230 Frankfurt (Oder)

SIGNATURE: _____ DATE: May 26, 1999

Silicon Germanium Hetero Bipolar Transistor for High Frequency Applications and Method of Fabricating the Epitaxial Individual Layers of such a Transistor.

The invention relates to a silicon germanium hetero bipolar transistor for high frequency applications and to a method of fabricating the epitaxial individual layers of a silicon germanium hetero bipolar transistor for high frequency applications.

Aside from using gallium arsenide for fabricating super high frequency transistors, silicon germanium hetero bipolar transistors, because of their lower fabrication costs, have found increased use in high frequency areas. The sequence of layers in such transistors generally consists of a silicon collector layer, a base layer of p-doped silicon germanium, and an emitter layer.

German laid-open patent specification 43 01 333 A1 describes a method of fabricating integrated silicon germanium hetero bipolar transistors in which a collector layer, a base layer, an emitter layer and an emitter connection layer are precipitated and doped at the same time in a single uninterrupted process. This method of fabricating transistors for high frequency applications suffers from the drawback that a further increase in the doping of the base with doping atoms would lead to an outdiffusion, i.e. a broadening of the base region, at a corresponding temperature. Outdiffusion of dopants, on the one hand, results in a non-uniform fabrication of transistors and, on the other hand, in a reduction of collector and emitter currents. Accordingly, it is not possible by this method to improve the high frequency

properties of transistors. Also, broadening of the doped regions limits a further reduction of the structure.

Japanese patent application JP 5,102,177 discloses a silicon germanium hetero bipolar transistor the base of which has been dislocated by 5 % of carbon to compensate for mechanical strain introduced by the germanium. However, such high carbon concentrations result in a strong local lattice deformation which limits the suitability of such transistors for high frequency applications.

Also, in IEEE Electron Device Letters, Vol. 17, No. 7, July 1996, pp. 334-337 as well Appl. Phys. Lett., vol. 60, No. 24, pp. 3033-3035, 1992 and Meter. Lett., Vol. 18, pp. 57-60, 1993, carbon is incorporated into the base for the purpose of attaining current compensation of germanium in silicon by carbon as well as a variation in the band gap. Optimum results were found at a carbon concentration of $5 \cdot 10^{20}$ cm^{-3}. Drawback similar to those of the above-mentioned JP 5,102,177 may be expected. In IEEE Electron Device Letters, Vol. 17, No. 7, July 1996, pp. 334-337, large surface MESA transistors with emitter surfaces of ≥ 400 μm^2 (line width ≥ 20 µm) were used to define static component properties. Such transistors with large emitter surfaces do not satisfy high frequency applications.

To fabricate SiGe transistors suitable for high frequency applications line widths less than 2 µm are necessary as disclosed, for instance, in T.F. Meister: SiGe Base Bipolar Technology with 74 Ghz f_{max} and 11 ps Gate Delay; IEDM95-739.

U.S. patent 5,378,901 discloses a silicon carbide transistor in which silicon carbide is used as the material for the base, collector and emitter. The high fabrication temperatures prevent their integration into circuits suitable for high frequency applications.

It is a task of the invention to provide a silicon germanium hetero bipolar transistor suitable for high frequency applications in which the outdiffusion of dopant from the base region is reduced by more than 50 % compared to conventional silicon germanium hetero bipolar transistors. It is a further task of the invention to structure known methods of fabricating the epitaxial individual layers of such silicon germanium hetero bipolar transistor suitable for high frequency applications with a silicon collector layer, a doped silicon germanium base layer and a silicon emitter layer so as to reduce the usual limitations and complex requirements of subsequent processes. This refers especially to the implantation dose and the temperature time stress of the epitaxial layer. Silicon germanium hetero bipolar transistors made by this method have a higher transitory frequency, an increased maximum oscillation frequency and/or a reduced noise level depending upon requirements and intended application.

Furthermore, it is a task of the invention by a point defect supported diffusion acceleration to prevent boron outdiffision from the silicon germanium layer, in order to attain HF properties without losses in a scaling range of a line width of .4 µm or less. In this manner, similar transitory and maximum oscillation frequencies are to be attained compared to larger emitter surfaces.

In accordance with the invention these tasks are accomplished by the invention described hereinafter.

A monocrystalline structure according to a desired transistor profile is precipitated on a surface of pure silicon. In at least one of its three individual layers, i.e. its emitter layer or its base layer or its collector layer, the silicon germanium hetero bipolar transistor in accordance with the invention contains an additional material which is electrically inert, preferably an element from group IV, in a concentration between 10^{18} cm^{-3} and 10^{21} cm^{-3}. The semiconductor arrangement of the silicon germanium hetero bipolar transistor

is fabricated by an epitaxy process, e.g. by vapor phase epitaxy or molecular-beam epitaxy. The technological process steps following the epitaxy lead to defects, e.g. interstitial atoms in the semiconductor crystal, which enhance the diffusion of atoms foreign to the lattice, such as dopants. An electrically inactive material of the kind referred to and incorporated into the epitaxial layer links these defects and reduces the diffusion of the dopant. The relative alteration of the lattice constant caused by the incorporation of an electrically inert material, preferably carbon, is less than $5 \cdot 10^{-3}$. The outdiffusion of the dopant is reduced which limits broadening of the base region. This allows fabrication of transistors suitable for high frequency applications in two ways: The dopant dose of the base region is increased and/or the width of the base is reduced. Either way leads to an increase in the concentration of dopant in the base region of the transistor by between $5 \cdot 10^{18}$ cm^{-3} and 10^{21} cm^{-3} if the dopant used is boron. This leads to a reduced resistance of the inner base. The invention proceeds on the basis of the conventional fabrication of a preprocessed silicon substrate. The method is characterized by the following process steps: Initially silicon is deposited by vapor deposition for fabricating the collector layer. Germanium is additionally incorporated during the following further silicon vapor deposition and is doped with lattice doping atoms. The preferred dopant used is boron. The base is fabricated by this process step. After discontinuing the addition of boron and the doping medium the emitter layer is fabricated by further vapor deposition of silicon.

During at least one of the mentioned process steps an electrically inert material, preferably carbon, is added in a concentration of between 10^{18} cm^{-3} and 10^{21} cm^{-3}, the relative change in the lattice constant thus introduced being less than $5 \cdot 10^{-3}$ owing to the low concentration of the electrically inert material. A low additional lattice distortion does not imply an additional source of possible lattice defects. CVD (chemical vapor deposition) and MBE (molecular-beam epitaxy) processes are used to fabricate the epitaxial layers. Conventional further processing is carried out terminating in the silicon

germanium hetero bipolar transistor in accordance with the invention. In silicon germanium hetero bipolar transistors in accordance with the invention the product of the germanium concentration in the base layer and the width of the base layer from the collector to the emitter is between 50 atomic percent·nm and 2,000 atomic percent·nm. The width of the base layer from the collector to the emitter is between about 5 nm and 60 nm and, preferably, between 35 nm and 40 nm. The concentration of germanium in the base layer is between about 8% and 30% and, preferably, between 20% and 28%.

The elements of the invention have not only been set forth in the claims but also in the description and in the drawings, whereby individual elements constitute patentable inventions not only by themselves but also when combines as subcombinations, the protection of which is here being applied for. Embodiments of the invention have been depicted in the drawings and will be described in greater detail hereinafter. In the drawings:

Fig. 1 is a schematic rendition of the layer structure of a silicon germanium hetero bipolar transistor;

Fig. 2 depicts steps of the method of fabricating the epitaxial individual layers of a silicon germanium hetero bipolar transistor;

Fig. 3 is a schematic section through a silicon germanium hetero bipolar transistor;

Figs. 4, 5, 6 depict concentration curves of germanium in silicon germanium hetero bipolar transistors.

In Fig. 1, there is shown the layer structure of a silicon germanium hetero bipolar transistor in accordance with the invention, consisting of a doped silicon substrate 1, a non-doped silicon carbon collector layer 2, a doped silicon germanium carbon layer 3 and a non-doped silicon carbon emitter layer 4. The entire layer structure including doping of the base region with boron is fabricated by molecular beam epitaxy.

In this embodiment, carbon in a concentration between 10^{18} cm^{-3} and 10^{21} cm^{-3} is added simultaneously with the epitaxy of all three individual layers, the collector layer, the base layer and the emitter layer. This corresponds to a carbon concentration of between .0015% and 1.5%. In this manner an otherwise possible diffusion of boron is significantly reduced so that the regions of dopant outdiffusion 5 may be reduced compared to conventional transistors of this kind. By the addition of carbon in accordance with the invention the diffusion length of boron is reduced by more than 50% compared to a diffusion length occurring where no carbon has been added. The result is a very stable boron profile. The thus reduced base width results in a reduced base transit time. This, in the context of the transistor in accordance with the invention, is the same as an increased transit frequency and an increased maximum oscillation frequency or a reduced noise level.

By increasing the boron concentration to between $5 \cdot 10^{18}$ cm^{-3} and 10^{21} cm^{-3} in the base layer the suitability of the silicon germanium hetero bipolar transistor may be further improved.

For fabricating such a silicon germanium hetero bipolar transistor the following process steps shown in Fig. 2 are performed: Prior to the part of the method in accordance with the invention a pretreated silicon substrate is conventionally made in a process step A_0. This is followed by the steps of:

A vapor deposition of silicon to fabricate the collector layer;

B Vapor deposition of silicon and additional incorporation of germanium and dopant for fabricating the base layer; and

C discontinuing germanium and dopant and vapor deposition for fabricating the emitter layer

whereby carbon in a concentration of between 10^{18} cm^{-3} and 10^{21} cm^{-3} is incorporated during at least one of the process steps with the relative change of the lattice constant thus introduced being less than $5 \cdot 10^{-3}$.

The epitaxy is followed by convention further processing D terminating in a final silicon germanium hetero bipolar transistor in accordance with the invention.

Fig. 3 depicts a schematic section through a silicon germanium hetero bipolar transistor thus fabricated. The non-doped silicon carbon collector 32, the non-doped silicon carbon emitter 33 and the base 34 of silicon, germanium and carbon doped with boron in a concentration between $5 \cdot 10^{18}$ cm^{-3} and 10^{21} cm^{-3} have been grown by epitaxy on the highly doped silicon substrate 31. Furthermore, the figure depicts the corresponding contact areas 35 as well as an implantation region 36. The carbon concentration in the epitaxial layer is between 10^{18} cm^{-3} and 10^{21} cm^{-3}.

Figs. 4 to 6 represent concentration curves of germanium in the silicon of silicon germanium hetero bipolar transistors in accordance with the invention. The curves are rectangular, triangular or trapezoidal. In all diagrams, the base region is limited on the abscissa by value x1 and x2. The ordinate represents the curve as a percentage of the germanium concentration.

In the transistor having the rectangular germanium concentration curve of Fig. 4 the width of the base layer is 30 nm. The concentration of germanium in the base layer is about 22% constant. Preferred high current amplifications and good dynamic properties may be obtained with this transistor profile.

In the transistor with the triangular germanium concentration curve of Fig. 5 the width of the base layer is 40 nm. The concentration of germanium in the center of the base layer where it reaches its maximum is about 26%. This transistor profile makes it possible to set very high early currents. Moreover, this transistor profile permits impressing a drift field for reducing the

base transit time of the minority carrier.

In the transistor with the trapezoidal germanium concentration curve of Fig. 6 the width of the base layer is 35 nm. The concentration of germanium in the base layer increases linearly from the side of the collector or emitter of the transistor from about 10% to 22%. In this embodiment, high current amplification as well as high early current and a drift field are attained for reducing the transit time of the base.

At increased scaling broadening of the contact regions is avoided by the prevention of boron outdiffusion by carbon so that HF properties are preserved without losses in the scaling range of a line width of .4 µm or less. Compared to larger structures the same transit and maximum frequencies are attained here at lower currents.

In the context of the present invention a silicon germanium hetero bipolar transistor suitable for high frequency applications and a method of fabricating the epitaxial individual layers of such a transistor have been described with reference to concrete embodiments. It is, however, to be noted that the present invention is not restricted to the details of the description of the embodiments as changes and alterations are claimed within the metes and bounds of the patent claims.

Patent Claims

1. Silicon germanium hetero bipolar transistor suitable for high frequency applications, with a silicon collector layer, a doped silicon germanium base layer and a silicon emitter layer, characterized by the fact that carbon is incorporated in at least one of the three individual layers, i.e. the emitter layer and/or the base layer and/or the collector layer, in a concentration between 10^{18} cm^{-3} and 10^{21} cm^{-3} and that the relative change in the lattice constant thus introduced is less than $5 \cdot 10^{-3}$ so that a point defect supported diffusion acceleration is prevented.

2. Silicon germanium hetero bipolar transistor suitable for high frequency applications according to claim 1, characterized by the fact that the base layer is doped with boron and with a concentration of the dopant in the base region between $5 \cdot 10^{19}$ cm^{-3} and 10^{-3} cm^{-3} the concentration of carbon in the epitaxy layer is between 10^{18} cm^{-3} and 10^{21} cm^{-3} and the defect density of the transistor is less than 10^{4} cm^{-2}.

3. Silicon germanium hetero bipolar transistor suitable for high frequency applications according to claim 1 or 2, characterized by the fact that the width of the base from the collector to the emitter is between 5 nm and 40 nm

4. Silicon germanium hetero bipolar transistor suitable for high frequency applications according to one or more of the preceding claims, characterized by the fact that the concentration of germanium in the base layer is between 8% and 30% and preferably between 20% and 28%.

5. Silicon germanium hetero bipolar transistor suitable for high frequency applications according to one or more of the preceding claims,

characterized by the fact that the shape of the germanium concentration curve corresponds to a rectangle, a triangle or a trapezoid.

6. Method of fabricating the epitaxial individual layers of a silicon germanium hetero bipolar transistor suitable for high frequency applications characterized in claim 1 with a silicon collector layer, a doped silicon germanium base layer and a silicon emitter layer, characterized by the fact that during fabrication of individual layers, i.e. the emitter layer (4), base layer (3) and collector layer (2) carbon is added to at least one of these layers in a concentration between 10^{18} cm^{-3} and 10^{21} cm^{-3} so that a point defect supported diffusion acceleration is prevented, and that the base layer is simultaneously doped with doping atoms with the relative change in the lattice constant thus introduced being less than $5 \cdot 10^{-3}$.

7. Method of claim 6, characterized by the fact that during one process step (A), namely vapor deposition of silicon for fabricating the collector layer, carbon is incorporated in a concentration between 10^{18} cm^{-3} and 10^{21} cm-3

8. Method of claim 6, characterized by the fact that during one process step (B), namely vapor deposition of silicon and additional incorporation of germanium and dopant for fabricating the base layer, carbon is incorporated in a concentration between 10^{18} cm^{-3} and 10^{21} cm^{-3}.

9. Method of claim 6, characterized by the fact that during one process step (C), namely discontinuing germanium and dopant and vapor deposition of silicon for fabricating the emitter layer, carbon is incorporated in a concentration between 10^{18} cm^{-3} and 10^{21} cm^{-3}, the

relative change in the lattice constant thus introduced being less than $5 \cdot 10^{-3}$.

10. Method according to one of claims 7 to 9, characterized by the fact that during process steps (A) and (B) or process steps (A) and © or process steps (B) and © carbon is incorporated in a concentration between 10^{18} cm^{-3} and 10^{21} cm^{-3}.

11. Method according to one or more of the claims 7 to 10, characterized by the fact that during fabrication of the base layer (3) boron is used as the dopant in a concentration between $5 \cdot 10^{18}$ cm^{-3} and 10^{21} cm^{-3}.

12. Method according to one or more of the claims 7 to 11, characterized by the fact that fabrication of the epitaxial layer is performed by a CVD process.

13. Method according to one or more of the claims 7 to 11, characterized by the fact that fabrication of the epitaxial layer is performed by a MBE process.

Abstract

The invention relates to a silicon germanium hetero bipolar transistor suitable for high frequency applications and a method of fabricating the epitaxial individual layers of a silicon germanium hetero bipolar transistor suitable for high frequency applications.

Silicon germanium hetero bipolar transistors thus fabricated have an increased transit frequency, an increase maximum oscillation frequency and/or a reduced noise level depending upon requirements and intended application.

A monocrystalline deposition is performed on a surface of pure silicon in accordance with the desired transistor profile. The silicon germanium hetero bipolar transistor contains an additional electrically inert material. The semiconductor arrangement of silicon germanium hetero bipolar transistors is fabricated by an epitaxy process. A electrically inert material incorporated into the epitaxial layer links fabrication defects and reduces the diffusion of the dopant. Thus, transistors for high frequency applications may be fabricated in two ways: The dopant dose of the base region is increased and/or the width of the base is reduced.

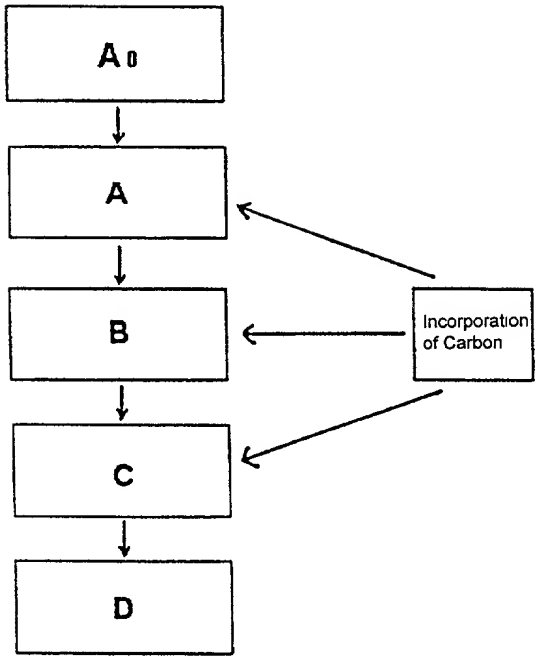

Fig. 2

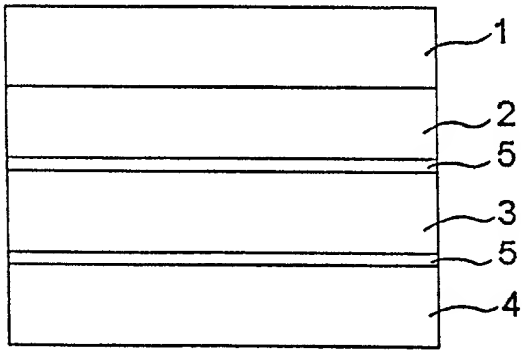

Fig. 1

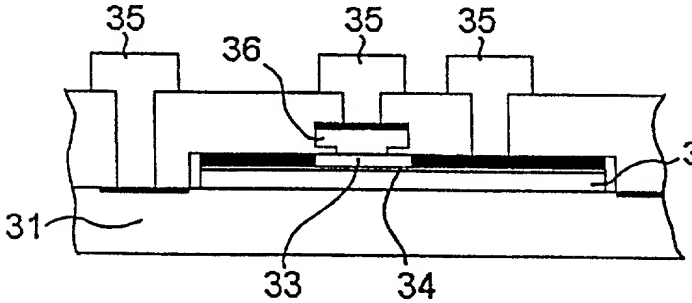

Fig. 3

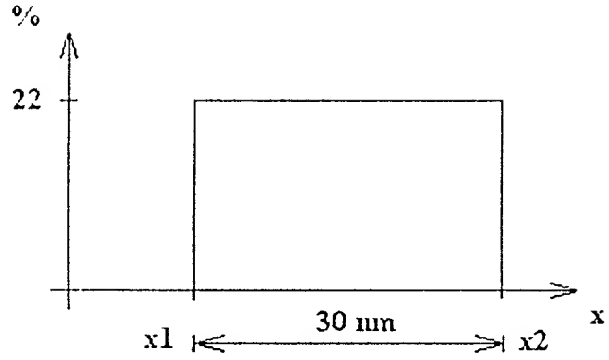

Fig. 4

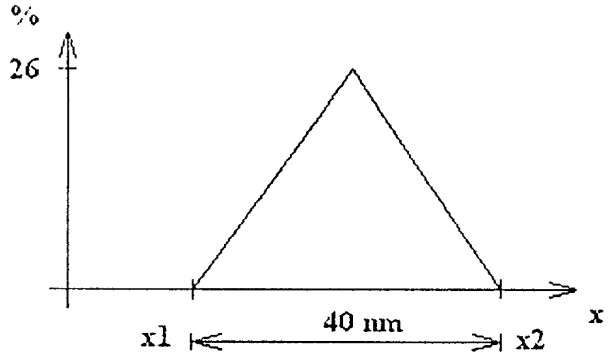

Fig. 5

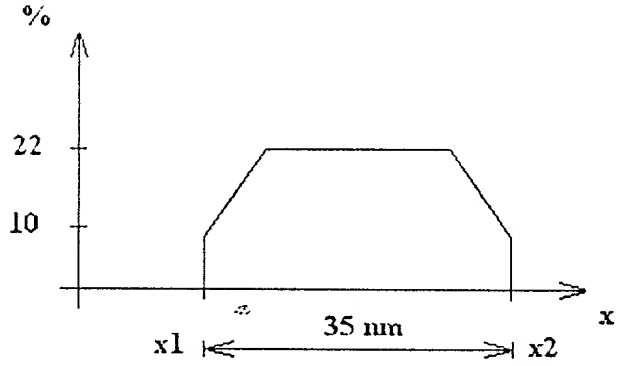

Fig. 6

Docket No.
990326

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Silicon Germanium Hetero Bipolar Transistor and Method of Fabricating the Epitactic Layers Thereof

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
196 52 423.7	**Germany**	**9 December 1996**	☐
(Number)	(Country)	(Day/Month/Year Filed)	
197 55 979.4	**Germany**	**6 December 1997**	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

N/A	
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

PCT/DE97/02908	8 December 1997	Pending
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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DEX

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Fifth inventor's signature

Date

Residence

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Post Office Address

Full name of sixth inventor, if any

Sixth inventor's signature

Date

Residence

Citizenship

Post Office Address